## REMARKS

This paper is being provided in response to the Final Office Action mailed September 9, 2004, for the above-referenced application. In this response, Applicant has amended claims 6, 9, 15, 17 and 18 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification.

Applicant notes that the Office Action Summary indicates with a checked box that "The specification is objected to by the Examiner." However, the text of the Office Action contains no description of any objection to the specification. Accordingly, Applicant respectfully requests that the specification be indicated as non-objectionable or further information be provided as to any objections that the Examiner may have.

The rejection of claims 6-11 and 15-25 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,100,118 to Shih (hereinafter "Shih") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 6, as amended herein, recites a semiconductor device. The device includes a substrate and a first dielectric film overlying the substrate, said first dielectric film having a pair of trenches formed therein apart from each other. A pair of fuse terminals are embedded in an associated one of said pair of trenches of the first dielectric film. A fuse element is formed on the second dielectric film in electrical contact with the pair of fuse terminals. An electrode pad is embedded in the first dielectric film having a conductive film disposed thereon.

A second dielectric film overlies the first dielectric film and covers the pair of fuse terminals. An opening is disposed in the second dielectric film that exposes at least a portion of the electrode pad and the conductive film. Claims 7 and 8 depend on independent claim 6.

Independent claim 9, as amended herein, recites a semiconductor device including a substrate. A first dielectric film overlies the substrate. A pair of fuse terminals are embedded in a surface portion of said first dielectric film. A fuse element is formed on the first dielectric film and connected to the pair of fuse terminals. An electrode pad is embedded in the first dielectric film and having a conductive film disposed thereon. A second dielectric film is formed to cover the first dielectric film and the fuse element. A third dielectric film is formed on the second dielectric film and an opening is formed in the third dielectric film to expose a part of the second dielectric film above the fuse element. A first opening is formed in the third and second dielectric films to expose at least a portion of the electrode pad and the conductive film. A second opening is formed in the third dielectric film to expose a part of the second dielectric film above the fuse element. Claims 10-11 depend on independent claim 9.

Independent claim 15, as amended herein, recites a semiconductor device including a substrate. A first dielectric film overlies the substrate. First, second and third trenches are formed in the first dielectric film apart from one another. First and second fuse terminals are embedded respectively in the first and second trenches of the first dielectric film. An interconnection line is embedded in the third trench of the first dielectric film. A fuse element is formed on the interconnection line in contact therewith. A fourth trench is formed in the first dielectric film apart from the first, second and third trenches. An electrode pad is formed in the

fourth trench of the first dielectric film and having a second conductive film disposed thereon. A second dielectric film is formed to cover the first dielectric film, said fuse element and said first conductive film. A first opening is formed in the second dielectric film that exposes at least a portion of the electrode pad and the second conductive film. Claims 16-25 depend directly or indirectly on independent claim 15.

The Shih reference discloses a method of fabricating a metal guard ring around a metal fuse and fuse opening. The fuse opening 88 penetrates through multiple film layers to the metal fuse 41 and fuse terminals 38A and 38B. The metal guard ring is formed around the fuse opening. (See Figure 3 of Shih.)

Applicant's present claimed invention recites at least the features of a semiconductor device that includes a pair of fuse terminals embedded in a first dielectric film in electrical contact with a fuse element and *an electrode pad embedded in the first dielectric film and having a conductive film disposed thereon*, and *a second dielectric film overlying said first dielectric film and covering said pair of fuse terminals, and an opening disposed in said second dielectric film that exposes at least a portion of said electrode pad and said conductive film*. (See, for example, Figure 8 and page 12, lines 2-23 of the present application.) Applicant has found that a semiconductor device as recited in the claims allows for finer patterning and higher integration and further allows a reduction in the number of fabrication steps for the fuse structure. (See, for example, page 8, line 20 to page 10, line 4 of the present application.)

Applicant submits that Shih does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Specifically, Figure 3 of Shih illustrates a fuse opening 88 that is formed through multiple dielectric films and exposes the fuse element 41 and fuse terminals 38A-38B. The element 42 identified in the Office Action as an electrode pad is covered by the multiple dielectric films as part of the metal guard ring around the fuse opening 88. There is arguably no conductive film disposed on the metal element 42 and no opening in the second dielectric film that exposes at least a portion of the element 42 or a conductive film disposed thereon.

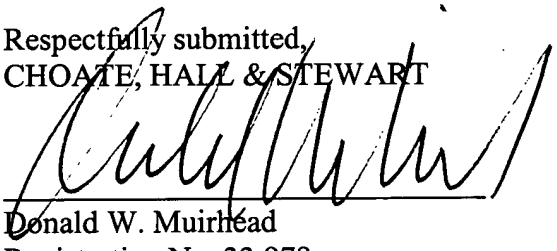
Accordingly, Applicant respectfully submits that Shih does not teach or fairly suggest at least the features of a semiconductor device that includes a pair of fuse terminals embedded in a first dielectric film in electrical contact with a fuse element and *an electrode pad embedded in the first dielectric film and having a conductive film disposed thereon*, and *a second dielectric film overlying said first dielectric film and covering said pair of fuse terminals, and an opening disposed in said second dielectric film that exposes at least a portion of said electrode pad and said conductive film*, as claimed by Applicant. In view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Furthermore, specifically with respect to claim 7, the Office Action cites Figure 3 of Shih as disclosing top interconnect lines formed as a common layer with fuse terminals (38A-B) and a protective film formed on said line body as a common layer with the fuse element (41). However, Applicants submit that the guard rings 139, 149, 159 (see Fig. 1 of Shih) are described by Shih as formed by the same metal layers used for configuring metal lines for devices in the

circuit areas (wiring areas) 86. (See col. 9, line 6 to col. 10, line 6 of Shih.) Consequently, Shih does not disclose a plurality of *top interconnect lines* configured as claimed by Applicant, because the interconnect lines of Shih that are cited in the Office Action are not the *top interconnect lines*. Accordingly, in addition to the reasons stated above with respect to independent claim 6, Applicant respectfully requests that the rejection of claim 7 be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
CHOATE, HALL & STEWART



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